The CMOS Inverter

Consider the **complementary MOSFET** (CMOS) inverter circuit:

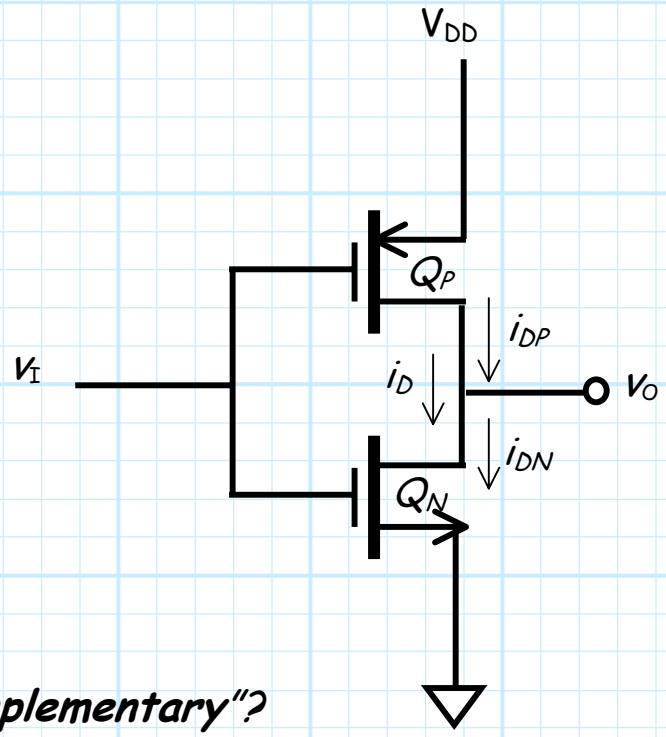
In this circuit:

$$i_{DP} = i_{DN} \doteq i_D$$

$$K_n = K_p \doteq K$$

$$V_{tp} = V_{tn} \doteq V_t$$

$$(V_{DD} > 2V_t)$$



Q: *Why do we call it "**Complementary**"?*

A: Because the device consists of an NMOS and PMOS transistor, each with **equal** K and equal but opposite V_t.

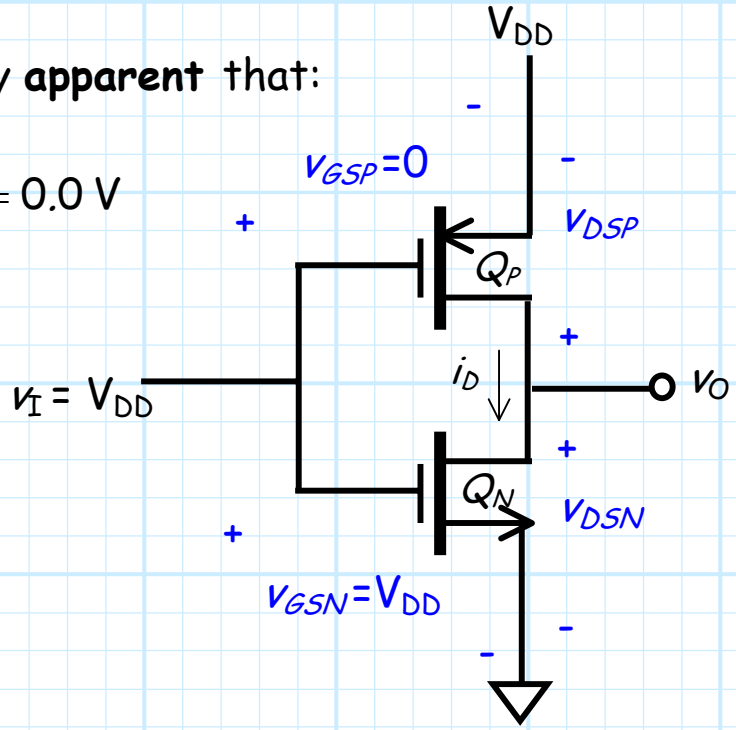
Q: *What makes the **CMOS** inverter so great?*

A: Let's **analyze** the circuit and find out!

First, let's consider the case where the **input** voltage is at the perfect "**high**" state $v_I = V_{DD}$.

For this case, it is readily **apparent** that:

$$v_{GSN} = V_{DD} \quad \text{and} \quad v_{GSP} = 0.0\ \text{V}$$



Hence, we can conclude:

$$v_{GSN} = V_{DD} > V_{tn} \quad \rightarrow \quad Q_N \textbf{ has} \text{ an induced channel !}$$

and:

$$v_{GSP} = 0.0\ \text{V} > V_{tp} \quad \rightarrow \quad Q_P \text{ has } \textbf{no} \text{ induced channel!}$$

Thus, we can conclude that Q_P is in **cutoff**, and Q_N is **either** in saturation or triode.

Let's ASSUME that Q_N is in **triode**, so we ENFORCE the condition that:

$$i_D = K_n \left[2\left(v_{GSN} - V_{tn}\right) v_{DSN} - v_{DSN}^2 \right]$$

Note that:

$$v_{GSN} = v_I = V_{DD} \quad \text{and} \quad v_{DSN} = v_O$$

Therefore:

$$\begin{aligned} i_D &= K_n\left[2\left(v_{GSN} - V_{tn}\right)v_{DSN} - v_{DSN}^2\right] \\ &= K\left[2\left(V_{DD} - V_t\right)v_O - v_O^2\right] \end{aligned}$$

Now, we actually KNOW that Q_P is in **cutoff**, so we likewise ENFORCE:

$$i_D = 0.0$$

Equating these two ENFORCED conditions, we find that:

$$i_D = 0 = K\left[2\left(V_{DD} - V_t\right)v_O - v_O^2\right]$$

Solving, we find that the **output** voltage must be **zero**!

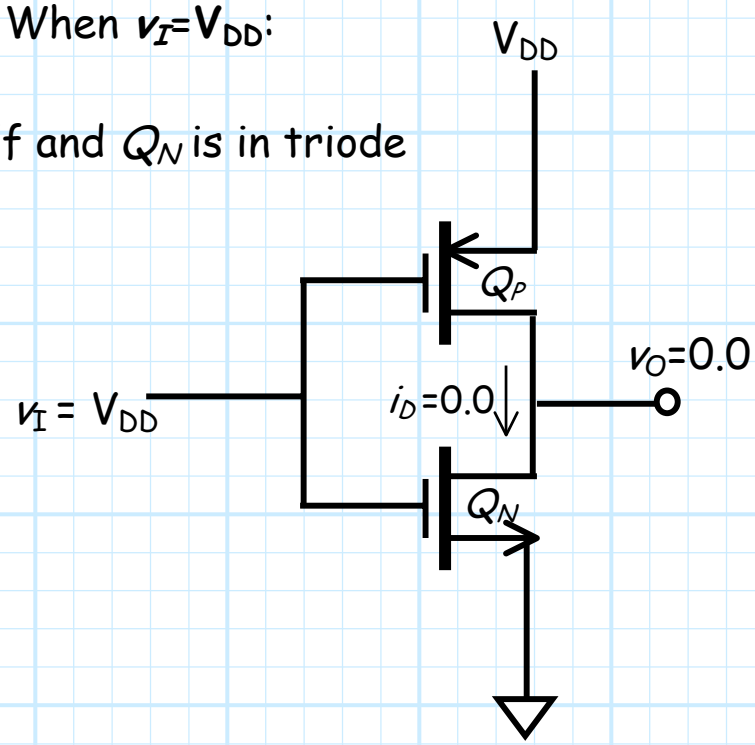
$$v_O = v_{DSN} = 0.0 \text{ V}$$

Thus, $v_{DSN} = 0 < v_{GSN} - V_{tn} = V_{DD} - V_t$. ✓

Q_N **is** indeed in the **triode** mode!

So, let's **summarize**. When $v_I = V_{DD}$:

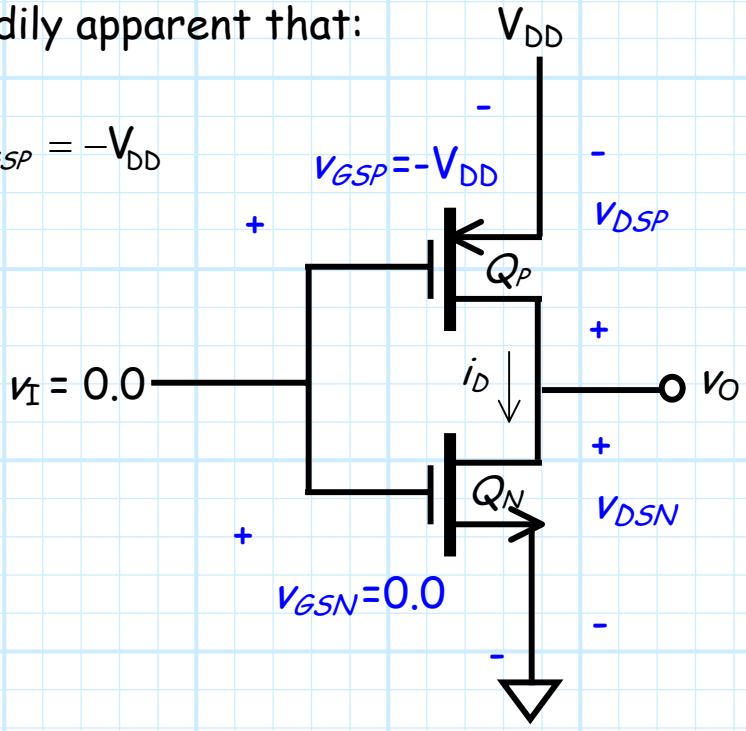
1. Q_P is in cutoff and Q_N is in triode
2. $i_D = 0.0$
3. $v_O = 0.0$



Now, let's consider the case where the **input** voltage is at the perfect "**low**" state $v_I = 0.0$.

For this case, it is readily apparent that:

$$v_{GSN} = 0.0 \quad \text{and} \quad v_{GSP} = -V_{DD}$$



Hence, we can conclude:

$$v_{GSN} = 0.0 < V_{tn} \quad \rightarrow \quad Q_N \text{ has } \textbf{no} \text{ induced channel !}$$

and:

$$v_{GSP} = -V_{DD} < V_{tp} \quad \rightarrow \quad Q_P \textbf{ has} \text{ an induced channel!}$$

Thus, we can conclude that Q_N is in **cutoff**, and Q_P is either in saturation **or** triode.

Let's ASSUME that Q_P is in **triode**, so we ENFORCE the condition that:

$$i_D = K_p\left[2\left(v_{GSP} - V_{tp}\right)v_{DSP} - v_{DSP}^2\right]$$

Note that:

$$v_{GSP} = v_I - V_{DD} = -V_{DD} \quad \text{and} \quad v_{DSP} = v_O - V_{DD}$$

Therefore:

$$\begin{aligned} i_D &= K_p\left[2\left(v_{GSP} - V_{tp}\right)v_{DSP} - v_{DSP}^2\right] \\ &= K\left[2\left(V_t - V_{DD}\right)\left(v_O - V_{DD}\right) - \left(v_O - V_{DD}\right)^2\right] \end{aligned}$$

Now, we actually KNOW that Q_N is in **cutoff**, so we likewise ENFORCE:

$$i_D = 0.0$$

Equating these two ENFORCED conditions, we find that:

$$i_D = 0.0 = K\left[2(V_t - V_{DD})(v_O - V_{DD}) - (v_O - V_{DD})^2\right]$$

Solving, we find that the **output** voltage must be V_{DD}!

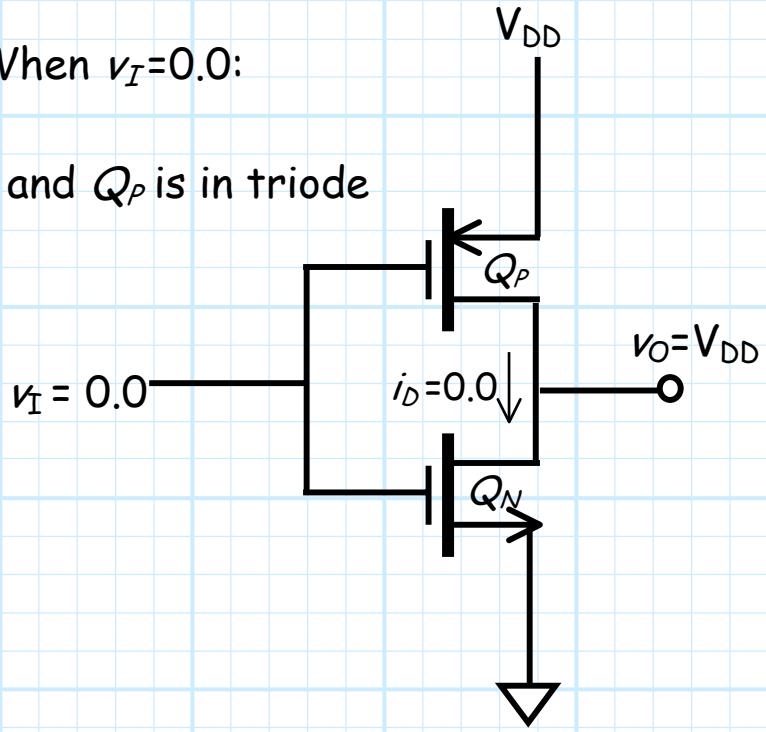
$$v_O = V_{DD}$$

Thus, $v_{DSP} = 0 > v_{GSP} - V_{tp} = V_t - V_{DD}$. ✓

Q_P **is** indeed in the triode mode!

So, let's **summarize**. When v_I=0.0:

1. Q_N is in cutoff and Q_P is in triode
2. i_D=0.0
3. v_O=V_{DD}



So, the overall behavior of the CMOS inverter is displayed in this **table**:

v_I	v_O	i_D
0.0	V_{DD}	0.0
V_{DD}	0.0	0.0

Look at what this means! The CMOS inverter provides **lots** of **ideal** inverter parameters:

$$V_{OL} = 0.0 \text{ V} \qquad \text{(ideal!)}$$

$$V_{OH} = 5.0 \text{ V} \qquad \text{(ideal!)}$$

And since i_D is **zero** for either state, the **static power** dissipation is likewise **zero**:

$$P_D \text{ static} = 0.0 \quad \text{(ideal!)}$$

This is one of the **most attractive** features of **CMOS** digital logic.